Power-over-Ethernet Interface PD Controller Meets IEEE802.3af™ Standard

Features

- Implements IEEE802.3af standard for PD
- 400mA inrush current limit
- 350mA operating current
- 400mA fault current limit
- Fast response current limit when over current or step voltage at input supply
- Programmable UVLO/ENABLE pin
- 9 seconds auto restart
- Built in thermal shutdown with hysteresis
- 90V open drain $\overline{\text{PWRGD}}$ (active low) output.
- Optional turn on time out disable
- On board 90V, 1W MOSFET
- Input voltage surge ratings up to 90V
- IOL tested

Applications

- IP phones
- Wireless access points
- End-spans and mid-spans
- PoE routers, switches
- Chargers
- Security peripherals & cameras

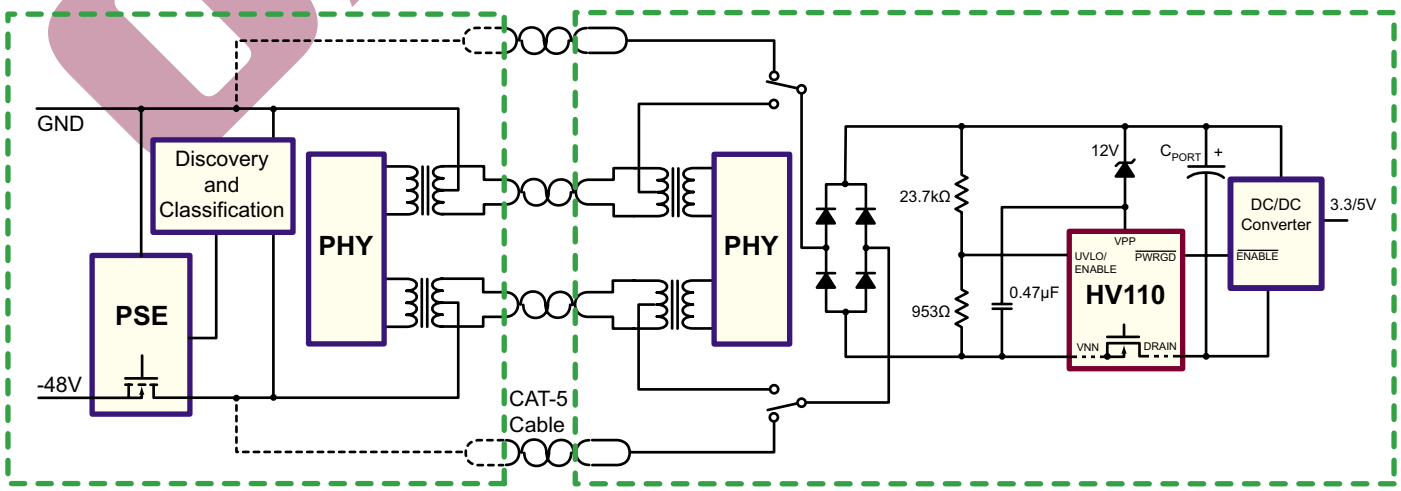
General Description

The HV110 provides complete power management and protection for Powered Devices (PDs) utilizing the IEEE802.3af protocol. As the most complete PD Power Manager available, the HV110 features a 400mA inrush limit and fault current limit, as well as minimum current shutdown to ensure additional protection and reliability to expensive equipment connected to the PD switch. The internal power switch uses scaled current-mirror technology, which eliminates the need for an external sense resistor and provides highly accurate current sensing at the high and low end operating conditions.

The HV110 uses a rugged high voltage junction isolated process, which eliminates the need for any external high voltage protection devices at the input of these controllers. Circuit isolation also reduces the chance of tripping on system noise. A 90V open drain $\overline{\text{PWRGD}}$ pin provides status information and can be used to enable the DC/DC power supplies.

The HV110 is available in a thermally rugged 5-Lead D-PAK package that provides improved thermal resistance when compared to 8-Lead SOIC based solutions.

Typical Application Circuit



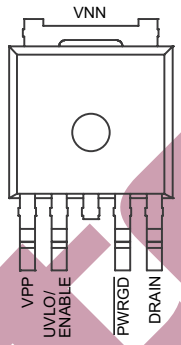
Note: A decoupling capacitor may be connected across VPP and VNN pins when used with long CAT-5 cables.

Ordering Information

Device	Package Option
	5-Lead TO-252 (D-PAK)
HV110	HV110K4-G

-G indicates package is RoHS compliant ('Green')

Pin Configuration



5-Lead TO-252 (D-PAK) (K4)

Absolute Maximum Ratings

Parameter	Value
Supply voltage, V_{PP} [1]	-0.5V to +90V
Operating temperature range	-40°C to +85°C
Storage temperature range	-65° to +150°C
5-Lead D-PAK thermal resistance $R_{\theta ja}$ (minimum footprint)	110°C/W
UVLO/Enable input[1]	6.0V
$\overline{\text{PWRGD}}$ open collector input[1]	90V

Absolute Maximum Ratings are those values beyond which damage to devicemay occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level my affect reliability. All voltages are references to VNN pin.

Note:

1. *The HV110 will work in both positive and negative voltage applications, the maximum differential voltage between the VPP and VNN pins must not be exceeded.*

Pin Description

Pin	Function
VPP	Positive voltage supply input
VNN	Negative voltage power supply input
DRAIN	Internal N-channel MOSFET drain output
UV/ENABLE	Under voltage lockout input
$\overline{\text{PWRGD}}$	Active-low power good output

Product Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____= "Green" Packaging

5-Lead TO-252 (D-PAK)

Electrical Characteristics *(at 0°C < T_A < +75°C, unless otherwise specified)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{PP}	Supply voltage[1]	36	-	57	V	V_{PP} referenced to V_{NN}
I_{PP}	Supply current	-	-	1.0	mA	V_{PP} = -48V, standby mode. MOSFET off.
V_{UVLO}	Internal UVLO threshold (turn-off)[2]	30	32	34	V	V_{PP} referenced to V_{NN}
V_{UVHO}	Internal UVLO threshold (turn-on)[2]	38	40	42	V	V_{PP} referenced to V_{NN}
V_{HYS}	UVLO comparator hysteresis	-	8.0	-	V	---
V_{UVTH}	UVLO comparator threshold	1.1	1.2	1.3	V	Referenced to V_{NN}
R_{UVLO}	UVLO input resistance	-	100	-	kΩ	---
R_{DS}	MOSFET on-resistance	-	1.0	1.6	Ω	Measured at 25°C and I_{DS} = 200mA
I_{LEAK}	Output leakage current	-	-	10	µA	Internal MOSFET off
I_{OUT}	Operating output current	-	-	350	mA	---
I_{INRUSH}	Inrush current limit	300	350	400	mA	---
I_{OC}	Over load current limiting	300	350	400	mA	---
I_{MIN}	Minimum current threshold	1.0	10	20	mA	---
V_{SLEW}	Slew rate to enable turn-on timers	-	4.25	-	V/ms	Enables timers

Notes:

1. *The HV110 will work in both positive and negative voltage applications, the maximum differential voltage between the VPP and VNN pins must not be exceeded.*
2. *UVLO Threshold to be modified using external resistors, when a Zener diode is connected to VPP pin. (See Signature Detection)*

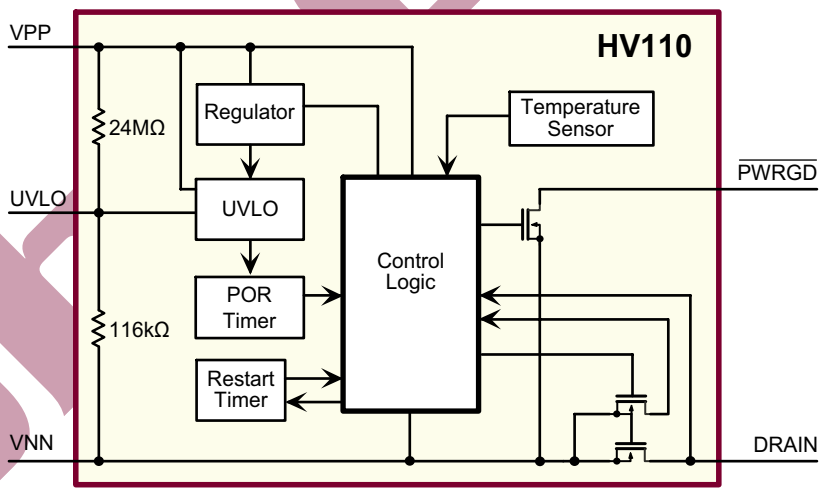
Electrical Characteristics *(cont.) (at 0°C < T_A < +75°C, unless otherwise specified)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
VOL_{PWRGD}	$\overline{PWRGD}$ output low voltage	-	-	0.4	V	I = 3.0mA; Referenced to V_{NN}
IOH_{PWRGD}	$\overline{PWRGD}$ output leakage current	-	-	10	µA	V = 5.0V; Referenced to V_{NN}
t_{SC}	Shorted-circuit timer[3]	-	60	-	ms	Measured at T_A = 25°C
t_{UC}	Under-current timer[4]	-	350	-	ms	Measured at T_A = 25°C
t_{OC}	Over-current timer[5]	-	60	-	ms	Measured at T_A = 25°C
t_{LIMIT}	Current limit delay time[6]	-	10	-	µs	Measured at T_A = 25°C
t_{POR}	POR timer	-	3.5	-	ms	Measured at T_A = 25°C
$t_{RESTART}$	Restart timer	-	9.0	-	sec	Measured at T_A = 25°C
T_{OT}	Over temperature trip limit	-	140	-	°C	---
T_{HYS}	Temperature hysteresis	-	20	-	°C	---

Notes:

1. *The HV110 will work in both positive and negative voltage applications, the maximum differential voltage between the VPP and VNN pins must not be exceeded.*
2. *UVLO Threshold to be modified using external resistors, when a Zener diode is connected to VPP pin. (See Signature Detection)*
3. *Shorted-circuit timer starts after POR timer. If V_{OUT} does not charge at least 90% V_{IN} before t_{SC} then a shorted-circuit condition exists.*
4. *Under-current timer starts when I_{OUT} goes below I_{MIN}. If I_{OUT} stays below I_{MIN} longer than t_{UC} then MOSFET is turned off due to under current condition.*
5. *If the output current is in an overload or shorted load condition then the output immediately goes to current limit and starts the over-current timer. If I_{OUT} does not drop back below I_{LIMIT} before the timer expires then an over current condition exists. The timer is immediately reset when a fault is cleared.*
6. *Time for fast return to limit circuit to react.*

Functional Block Diagram



Powered Ethernet Requirements

Power-over-LAN (sometimes called Powered Ethernet or Powered VoIP) is the general concept of providing high voltage (48VDC) power over existing networking cables, such as Ethernet cables. This is accomplished either by using the CAT5 Ethernet Cable's unused spare pairs or the signal pairs (ENV B vs. ENV A).

In Power-over-LAN applications there are two main types of equipment: the Power Sourcing Equipment (PSE) and the Powered Device (PD). There is a third type called Mid-Span equipment that plugs in line and converts a conventional router into a PSE.

The IEEE802.3af standard specifies the requirements, features and characteristics of the PSE and PD devices for use in PoE applications. The HV110 is a PD controller IC, capable of handling all the current and timing requirements of the IEEE802.3af standard.

A PD designed to this standard and within its range of available power, can obtain both power and data for operation via the standard LAN cables and therefore will not require any additional power sources or connections.

Power-over-Ethernet (PoE) Standards

IEEE802.3af standard, DTE Power via MDI, deals with the specification of the interface that can supply/draw power using the same generic cabling as that used for data transmission. It allows both power and data to flow through the Media Dependent Interface (MDI) (like 10Base-T, 100Base TX or 1000BaseT) to the Data Terminal Equipment (DTE) safely and effectively. It defines the functional and electrical characteristics of two optional power (non-data) entities – the Powered Device (PD) and the Power Sourcing Equipment (PSE) that makes this single interface possible. The mechanical and electrical interface between PSE and PD and the transmission line is achieved through the Power Interface (PI) Devices (usually the LAN cables).

PSE is defined as a device that provides a single portion of the link (10BASE-T, 100BASE_TX or 1000BASE_T) with both the data it requires and the power to process this data. PSEs may be placed with the DTE/Repeater/Mid-Span. A PSE that is located along with the DTE/Repeater is called Endpoint PSE, while a PSE that is located within the link, between the MDIs is called a Mid-Span PSE. All the specifications for the PSE sitting in the End Point (e.g. the router) may not apply for the Mid span PSE.

Even though the HV110 is a PD device, it is closely associated with the operation of PSE, in fact it is dependent on the PSE for its normal operation. The HV110, however, unlike many other PD controllers, provides redundant PSE protections and timings for maximum protection while ensuring compliance. Hence certain basic functionalities of the PSE are included in this data sheet for better understanding some of the features and operation of PDs.

PSE Power Standards

PSE powers a single link. It searches the link for a PD and supplies power to the link only after a PD Signature is detected. The PSE will reject any links with an invalid PD Signature. When the PD is removed, the PSE will also remove the power from the link.

PSE may be able to do an optional classification of the PD, to detect the maximum power drawn by the PD, to do some high level Power Management. PSE is limited to a continuous maximum output of 15.4W.

Discovery

Key to all Power-over-Ethernet methods is discovery. Discovery is the method used to determine if a device at the end of the cable is capable of receiving high voltage DC, before applying high voltage. Discovery also is used for determining when a PD device is disconnected or removed subsequently. The reason for all of this is that high voltages (-48V) connected to many legacy devices can cause equipment damage. For this reason discovery takes place at voltages compatible with existing legacy equipment and high voltage DC is only applied once discovery is satisfied. The IEEE802.3af discovery is based upon the sensing of a characteristic impedance. This impedance is defined nominally as 25k (23.5k to 26.25k) with no more than 0.1µF of capacitance in parallel with the impedance, in a voltage range from 2.8V to 10V. The presence of diode rectification at the PD end forces a slope impedance method, requiring at least two operating point measurements, to eliminate the effect of diode level shift.

Classification (optional)

As per the IEEE802.3af standards, the PSE has to deliver a minimum of 15.4W to a PD connected to it while limited by the 350mA maximum operating current. Not all PD devices, however, require this much power to operate. For example an IP Phone with a monochrome screen will require far less power than an IP Phone with color display. By identifying the power drawn through each port, PSE can assist in the System Power Management protocol to determine the total number of PDs it can support, depending on the output capacity of the system power supply.

To achieve this type of power management an optional step was added to the IEEE802.3af standard called 'Classification'. Classification allows a device to communicate the maximum power it will ever demand to the PSE so that the Power Management Protocol can allocate the unused power to other ports, enabling the full utilization of the installed capacity. Table 1 identifies the different Classifications included in the IEEE802.3af standard.

Table 1. PD Power Classification

Class	Usage	PD Power (W)
0	Default	0.44 – 12.95
1	Optional	0.44 – 12.95
2	Optional	3.84 – 6.49
3	Optional	6.49 – 12.95

In order to identify the class of the PD connected, the PSE sends a second voltage signal of 15 to 20V, slightly higher than signature detection voltage and measures the current. Depending on the magnitude of the current drawn, the PSE will classify the load to one of the four Classes as shown in Table 2, and will assume that the load will not draw any additional power than shown for the given Class.

Table 2. Classification signature measured at PD connector

Class	Probe Voltage (V)	Min (mA)	Max (mA)
0	15 - 20	0.5	4.0
1	15 - 20	9.0	12
2	15 - 20	17	20
3	15 - 20	26	30

Note that Class 0 default will work for all devices & Classification is only needed in the rare instance when a multi-port switch or router wants to rate the system supply lower than the combined Class 0 port output; a situation which will reduce it's potential classification base. In fact most of the PD devices, like Wireless Access Points, in the market today are Class 0 devices and hence do not require any classification methods. The HV110 therefore does not force the use of resistors and wasted silicon area to implement a Classification current source. The HV110, however, can be made to be compatible with classification by utilizing low cost circuitry as shown on page 6.

Disconnect

The PSE must be able to remove the power from a port once the PD is removed. The purpose of this is to prevent damage to non-compatible devices connected to the same link at a later time. As per the DC disconnect requirements, the PSE may disconnect load if the current is between 5mA and 10mA and must disconnect between 0-5mA, if the condition persists for more than 300ms. Although not required by a PD device, the HV110 includes a "minimum circuit breaker" which when the current is in a range less than 20mA will cause a shutdown after the 300ms if the PSE does not react.

PD Power Standards

According to the IEEE802.3af standards, the PD must operate from 36V to account for a potential 8.0V line drop across the impedance of the network during inrush (400mA max current x 20W line-impedance). The UVLO must allow a 44V max turn-on and a 30V minimum turn off. A PD device may draw a maximum power of 12.95W. The maximum power that can be expected is limited by the 20W line resistance carrying the 350mA current to the PD at the minimum input voltage of 44V (power delivered is 12.95W [{44 – (20*0.35)}*0.35].

PD Application

IEEE Electrical & Timing Requirements

Below are of the major features of the HV110, some of which are usually found only in PSE devices.

- Provides an internal current limit for inrush, normal operation and overload conditions.
- Limits the input current to less than 10µA that will not interfere with Discovery from 2.6V to 10V (with Zener as shown on page 1).
- Meets the turn-on and turn-off thresholds for the PD device & has a built-in 8.0V hysteresis (with PNP transistor as shown on page 9).
- Protects the device from thermal run away, with thermal shut down and built in 9 sec restart timer.
- UVLO & POR provides hot-swapping/de-bounce capabilities and inrush current limit.
- $\overline{\text{PWRGD}}$ (active LOW) provides enable signal to DC/DC converter.
- Complies with the timing requirements for IEEE 802.3af standard.
- Classification can be easily implemented, as shown on page 9.

In addition to operating as a PD controller, the HV110 can function as a redundant protective element to assure reliable operation and compliance to IEEE802.3af standard for the PD, even in cases where the PD is powered from an auxiliary power source, as shown on page 10.

Thermal Shutdown

The HV110 is designed with a built in Thermal Shutdown feature to assure higher levels of reliability. It will shutdown if the temperature on the die reaches 140°C and will try to restart when the temperature drops to 120°C.

Auto Restart

Any fault condition will cause the device to shut down and enable a 9 second auto-restart timer. This will occur indefinitely and is strong protection against PSE error when the the HV110 is used in PD applications.

Note that a 9 second auto-restart will disconnect the PD due to under current conditions, and will also turn off the PSE, since the PSE will not see the minimum current for greater than a period of 400ms (350ms nominal).

$\overline{\text{PWRGD}}$

The $\overline{\text{PWRGD}}$ (active low) pin is an open drain active low MOSFET, (referred to VNN) which is enabled when the gate voltage on the internal power MOSFET reaches its full on voltage, provided that the slew rate (V_{SLEW}) timeout for large capacitor is not being used.

Any fault condition will return $\overline{\text{PWRGD}}$ to a high impedance state, turning off the HV110 and the DC/DC converter. The PSE will also detect an undercurrent condition for a period greater than 350ms (nominal), and will shut down by itself. It will then wait for the next Discovery cycle.

Programmable UVLO and Hysteresis

ULVO is internally set through a 2.5MΩ and 116K resistance divider in the HV110. The default values of UVLO are given in the Electrical Characteristics on page 2.

The UVLO circuit has a built in Hysteresis of 8.0V, to enable stable operation during a UV condition. See the section on Signature Detection for further details.

Internal MOSFET with Current Mirror

The HV110 includes an internal 90V, 1.0Ω MOSFET. The MOSFET current is mirrored to a current detect circuit within the chip, utilizing a proprietary Supertex algorithm and wastes almost no power. Elimination of a sense resistor, necessary with external power switches, means additional energy savings, providing higher power output. Use of an on-board FET and the thermal supervisor also leads to high reliability compared to ICs that use external FETs whose temperatures cannot be easily monitored.

PD Polarity

According to IEEE802.3af, PD shall be insensitive to the polarity of the power supply and shall be able to operate in Mode A and Mode B (cases when the power is transferred through the signal leads and spare leads). The connections to the 8-pin modulator jack are different for Mode A and Mode B, polarity on the pins can be different for Mode A.

Accommodating the different pin combinations and polarity are beyond the scope of the PD Controller IC, however these must be taken care of in the system design. One of the ways of ensuring the polarity protection is to use a small bridge rectifier in between the 8-pin connector terminal and the PD Controller.

Description of Operation

Signature Detection

During the Discovery process, the PSE applies a voltage as described in the Discovery section on page 4 and determines if there is a PD connected at the other end of the cable. The power loss across the 25KΩ signature resistor will be less than 120mW - less than 1% of the power delivered to PD. It is therefore not critical to disconnect the signature resistor after the PD detection. However, this can be easily accomplished by using a low cost bipolar transistor and resistors. Note that the resistance of the external circuit connected between the DRAIN and VPP pin of the HV110 should be greater than 500kΩ (in the 2.8 – 10V Discovery voltage range) for the signature detect to work properly (usually the case with active loads like DC-DC converters).

Because of the Zener diode connected to VPP pin, it will be necessary to modify the internal UVLO thresholds by using two external resistances as shown in pages 1, 9 and 10, to provide the UVLO turn-off and turn-on voltages to meet the IEEE 802.3af standard. These two resistors perform dual functions, UVLO voltage adjustments and also the Signature Detection function (i.e. represent the 25k impedance). Page 9 shows a different implementation using a PNP transistor which allows the use of the HV110's internal UV circuit.

Once the voltage exceeds 12V, the HV110 will turn on and begin drawing a quiescent current of 1mA typical.

Current Limit Functions

The HV110 monitors the drain voltage and the current in the load switch. During initial inrush if the drain does not move more than 90% of input voltage within a short-circuit timer period (t_{SC} = 60ms), then the device will conclude that a short circuit condition exists, will turn off the internal FET and try to auto-restart after a period of 9 seconds. If the initial inrush period ends within this period as per the IEEE802.3af standards then the internal FET is turned fully on to minimize its on resistance and the $\overline{\text{PWRGD}}$ pin will be pulled low, to the negative rail.

Figure 1 shows the turn on sequence of the HV110. Once Discovery is complete, the $\overline{\text{PWRGD}}$ will be high impedance. After the optional Classification is complete and UVLO is satisfied, the HV110 will provide a controlled turn on of the internal switch (90V, 1W Power MOSFET), limiting the inrush current maximum value of 350mA (nominal).

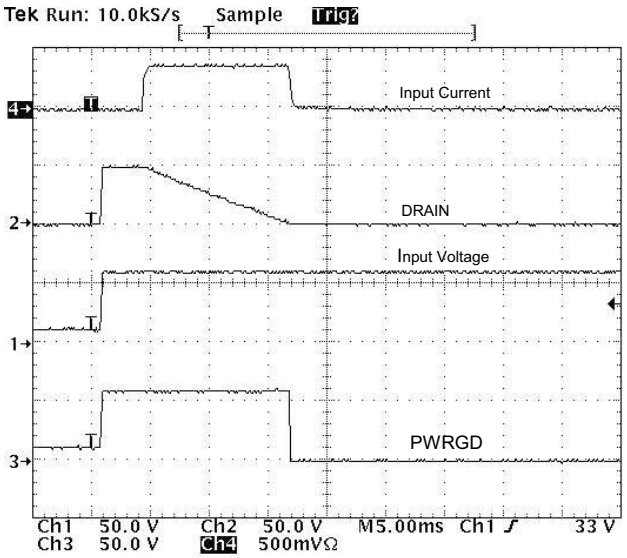


Figure 1. Turn-on waveforms of the HV110

During regular operation a fault condition can occur. The HV110 includes a current monitor that continuously watches the FET current. If the current exceeds 350mA (nominal), fast-return to limit feature will be activated and the over-current limit circuit will limit the output current to 350mA (nominal), as shown in Figure 2.

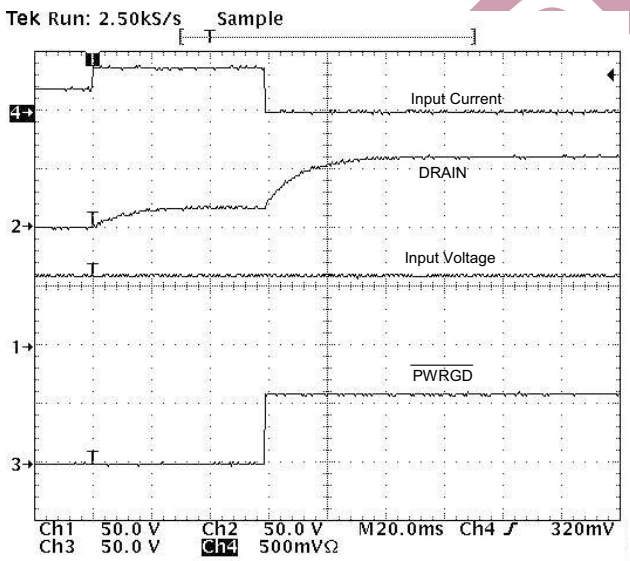


Figure 2. PD Current jumps from 200mA to 400mA, Controller shuts down in 60ms

If the fault is not cleared within the nominal over-current timer limit of 60ms, the HV110 will turn off the pass element, and initiate an auto-restart sequence, with a 9 second interval as shown in Figure 3. In the event the over-current is cleared before the over-current timer has expired, then the over-current timer will be reset and the device will start to function normally.

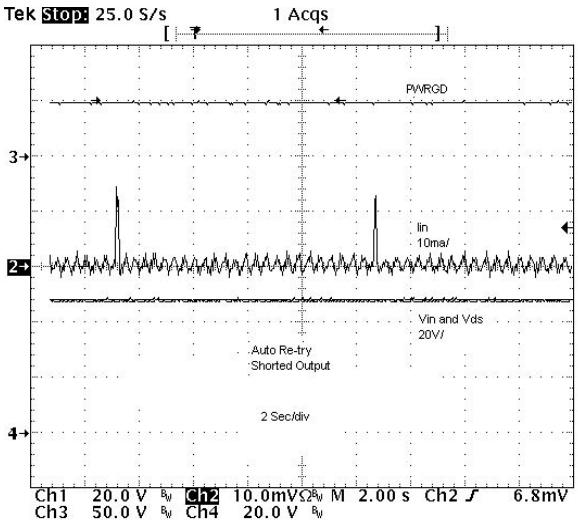


Figure 3. Auto-restart into a shorted output

DC Disconnect

The HV110 includes an under-current detection circuit to disconnect the PD when the current falls below the under-current threshold level. The HV110 will turn the internal FET off if the load current falls below a threshold level of 10mA (nominal) for a period determined by the under-current timer (signature drop-out time, t_{UC} 350ms nominal). In Class 0 applications, this acts as an additional protection to help overcome rapid reinsertion of a legacy or non-compliant device.

The HV110 provides most of the safety and timing requirements of a PSE in PoE applications hence can be considered as a secondary/redundant stage to comply with the IEEE 802.3af standards for the powered device. One motivation for this is that the PSE is an unknown quantity and may not be fully IEEE802.3af compliant in all cases. The HV110 will ensure that valuable PD devices are not damaged and that they fulfill the IEEE802.3af compliance.

Turning on to a large C_{PORT}

The PSE is required to limit the start up currents for C_{PORT} less than 180mF only, as per the IEEE802.3af standard. For higher value of C_{PORT}, the powered device has to limit the current. Figure 5 shows that the HV110 limiting current into 300mF as required by the IEEE802.3af specification.

To allow charging of extremely large capacitors, the HV110 includes a feature that will disable the turn on timers, $\overline{\text{PWRGD}}$ and Time out. This feature is based on the turn on voltage slew rate (V_{SLEW}). If V_{SLEW} is kept below 4.25V/ms then the timers are disabled and limiting will occur indefinitely until C_{PORT} is charged. This will also, however, disable $\overline{\text{PWRGD}}$ that is enabled by the same timer. In most cases the capacitor used in powered device application is well below 180µF so this feature is not of much significance in a powered device application.

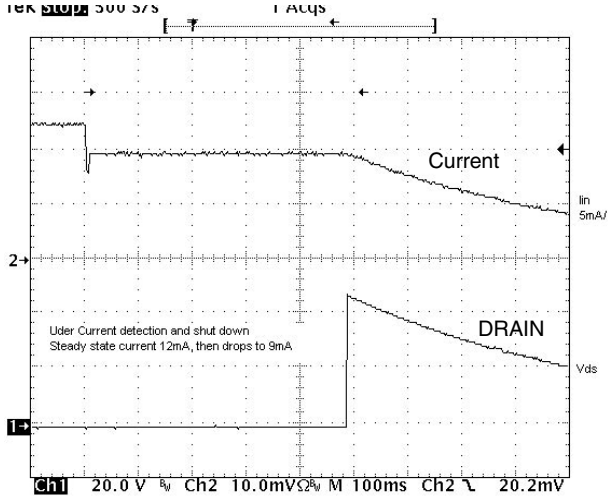


Figure 4. Undercurrent shutdown when current falls from 12mA to 9mA

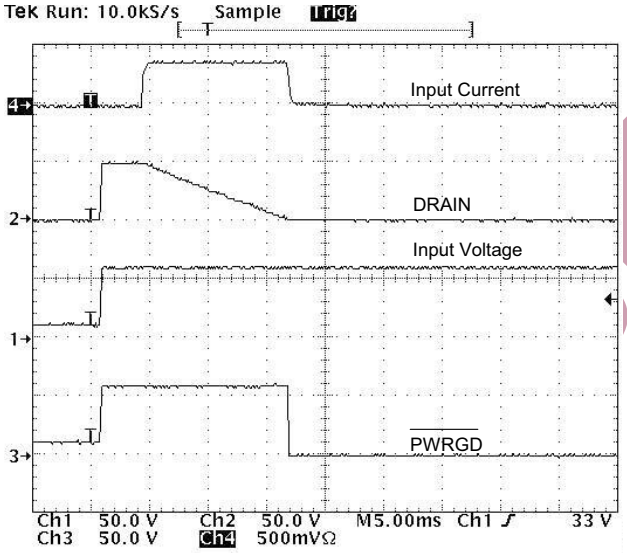


Figure 5. HV110 turning on into a 300uF C_{PORT}, still maintaining the maximum input current of 400mA (without any additional components required)

Application Circuits

Classification Option

Page 6 shows the schematic for a typical classification scheme used with the HV110. The PSE identifies the class of the powered device, by measuring the current flowing into R_{CLASS} during the classification period.

The reference voltage at the base of the bipolar transistor (the Zener and resistor) should be chosen to draw much less than 1.0mA so it does not interfere with classification levels. The Zener temperature coefficient is negative (if chosen below 4.0V), and the V_{BE} temperature coefficient is negative, providing a first order temperature compensated reference across R_{CLASS}. The $(V_Z-V_{BE})/R_{CLASS}$ allows programming of the classification current.

Choose R_{CLASS} corresponding to the current level of the powered device load, using the formula:

$$R_{CLASS} = (V_Z-V_{BE}) / (I_{CLASS} - IQ - 17.5V / 25k^*)$$

where V_Z is the voltage rating of the Zener diode, V_{BE} is the voltage across the B-E junction of the bipolar transistor, I_{CLASS} is the classification signature current corresponding to the power rating of the powered device as shown in Table 2 and IQ quiescent current of the HV110 (1mA). (* signature resistance)

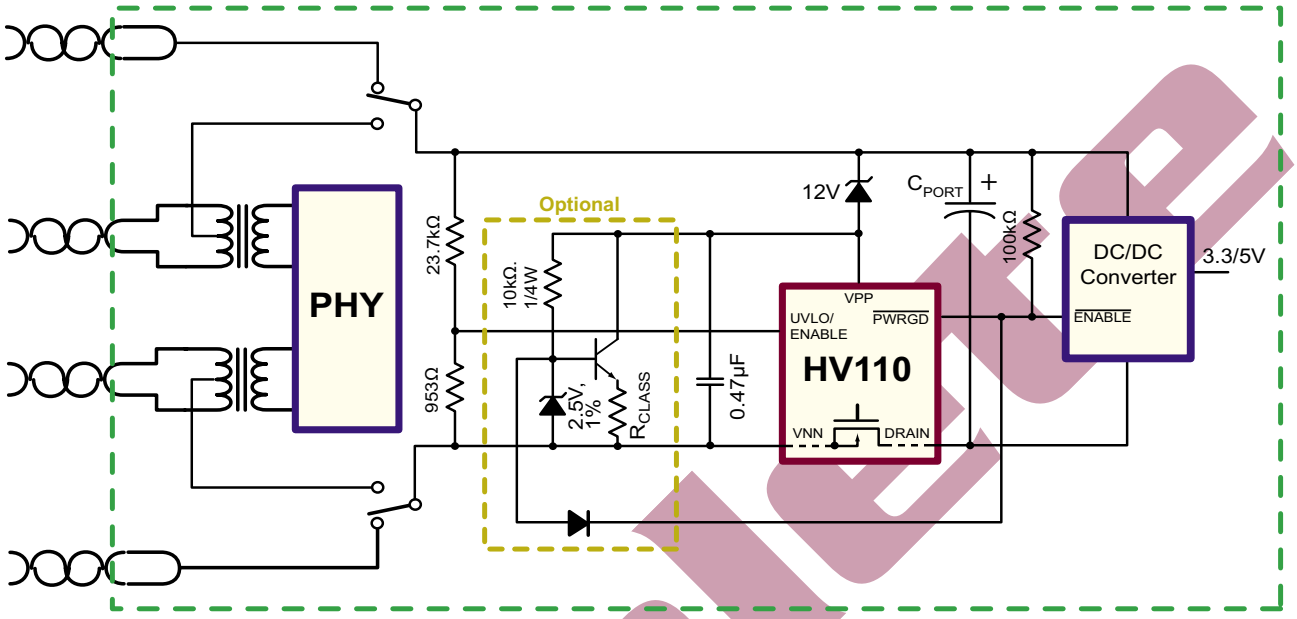
The above factors take into account the quiescent chip current above the 12V Zener voltage as well as the signature resistors in the mid-range of the classification probe voltage range. As the current ranges are wide, it is possible to ensure that the classification current is within the ranges of the Table 2 on Page 5 under all conditions. It is however recommended that a voltage reference be used instead of a Zener diode as the voltage reference will maintain the voltage across it over a wide current range.

The diode from base to $\overline{PWRGD}$ turns off classification as soon as $\overline{PWRGD}$ is pulled low to save power. The Zener in series with the HV110 will keep the classification components from drawing current until after Discovery. Make sure that the diode in series with the base of the bipolar transistor can block the maximum expected differential network voltage.

Table 3. R_{CLASS} for different classes of PD

CLASS	R_{CLASS}
0	Open
1	191Ω
2	95.3Ω
3	63.4Ω

Classification Circuit with the HV110

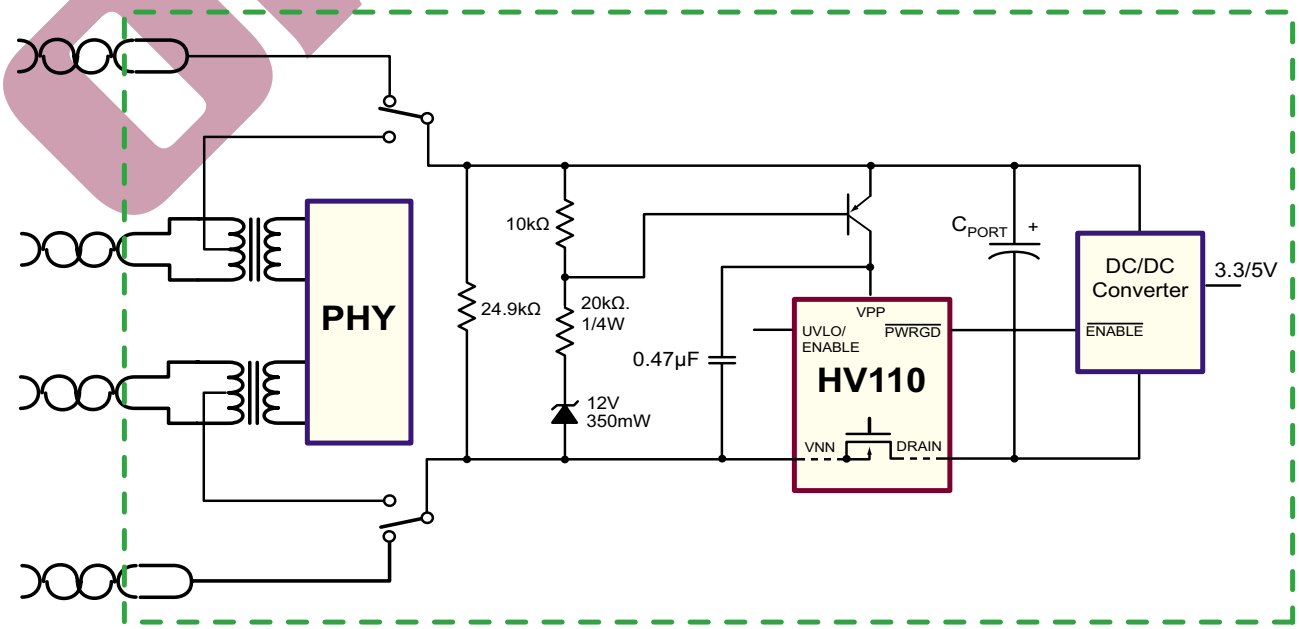


Alternate Method for Powering the HV110

The 12V Zener diode connected to the VPP pin of the HV110 (shown in Figure 1) is required to block the IC in the Discovery process, so that the quiescent current of the IC does not interfere with the signature resistance detect. However, this Zener causes a 12V drop across it, causing the HV110 to see only 36V. This makes the internal UV thresholds unusable. By using a PNP transistor along with a low power Zener and resistor instead, the built-in undervoltage thresholds can be utilized.

Figure 10 shows the modified circuit. In the Discovery stage, the input voltage is less than 10V. This causes the Zener to be reverse biased and hence there is no base current to the PNP transistor. Once the input voltage increases beyond 12V, the Zener starts conducting, which provides a base current path for the PNP transistor. The transistor goes into the saturation region, essentially pulling V_{PP} to the rail.

Powering the HV110 using a PNP transistor instead of a Zener

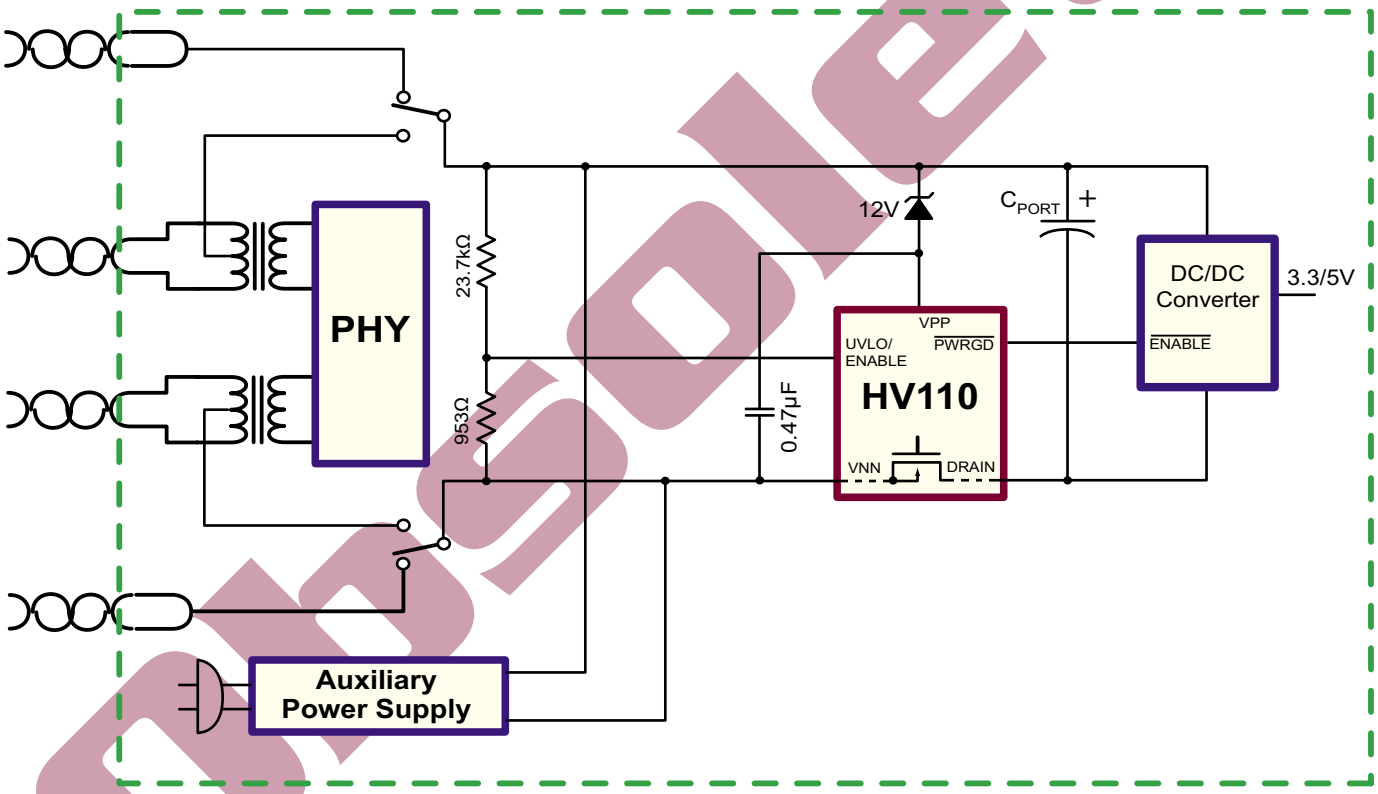


Operation with External Auxiliary Power Supply

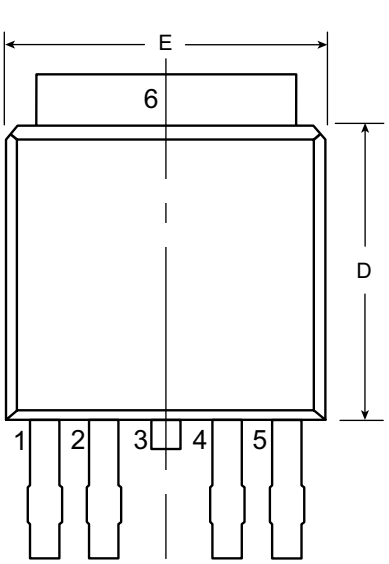
There may be cases when the powered device has to be powered by an external auxiliary power supply, when the powered device does not have a PSE at the other end of the Cat 5 cable. In such cases, the powered device can be powered by an external power supply as shown. By connecting the power source before connecting to the HV110 controller, the powered device will still operate correctly.

The higher voltage rating of the HV110 will address any voltage spikes up to 90V without the use of any external Zener diodes for input protection. The HV110 with its internal current limit and fault timing features will provide a reliable power source to the powered device and will allow the smooth transfer of data between the data terminal and the powered device. It may be necessary to connect a blocking diode to prevent any reverse current from being fed back into the cable to the remote side

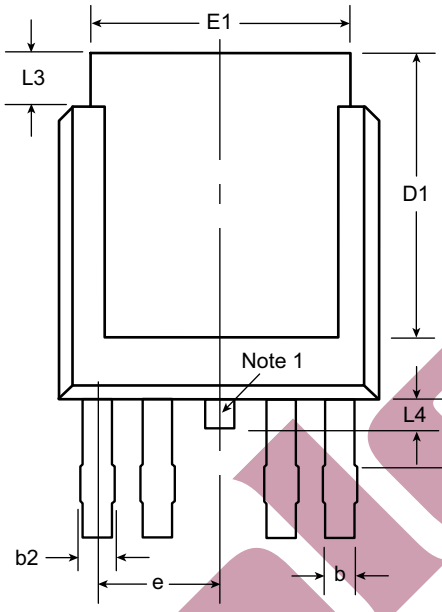
Powering HV110 from an Auxiliary power source



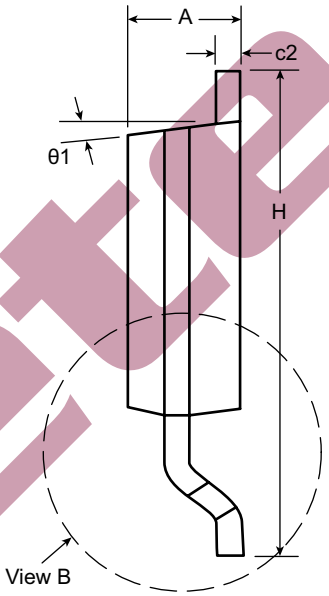
5-Lead TO-252 D-PAK Package Outline (K4)



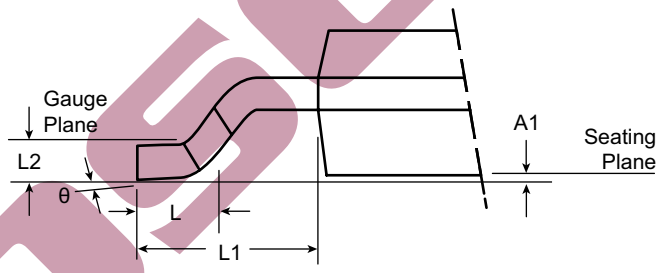
Front View



Rear View



Side View



View B

Note:

1. *Although 6 terminal locations are shown, only 5 are functional. Lead number 3 was removed.*

Symbol		A	A1	b	b2	c2	D	D1	E	E1	e	H	L	L1	L2	L3	L4	L5	θ	θ1
Dimen-sion (inches)	MIN	.086	-	.020	.024	.018	.235	.205	.250	.170	.045 BSC	.370	.055	.108 REF	.020 BSC	.035	-	.045	0°	0°
	NOM	-	-	-	-	-	.240	-	-	-		-	.060			-	-	-	-	-
	MAX	.094	.005	.028	.031	.035	.245	-	.265	-		.410	.070			.050	.040	.060	10°	15°

JEDEC Registration TO-252, Variation AD, Issue E, June 2004.
Drawings not to scale.
Supertex Doc. #: *DSPD-5TO252K4, Version B070308.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
TEL: (408) 222-8888 / FAX: (408) 222-4895
www.supertex.com

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Supertex:

HV110K4 HV110K4-G