July 11, 2011

C8051F50x-51x Errata

Errata Status Summary

This document summarizes all known errata with these devices.

Errata #	Title	Impact	Revisions A-B
1	Cold Programming Temperature on industrial grade (-I) parts only.	Minor	Issue exists
2	Long-reset Oscillator Lockup	Minor	Issue resolved from date code “1124”
3	P0.0 Open-Drain Mode	Minor	Issue exists

Impact Definition: Each erratum is marked with an impact, as defined below:

- Minor—Workaround exists.
- Major—Errata that do not conform to the data sheet or standard.
- Information—The device behavior is not ideal but acceptable. Typically, the data sheet will be changed to match the device behavior.

Errata Details

1. **Description**: For –I (Industrial Grade parts) a cold temperature programming deficiency may be present on weak Flash memory bits. There is no problem programming the Flash at 0 °C and above. There is only a potential Flash read issue if programming was done at cold temperature below 0 °C. If programmed at 0 °C or higher, there is no problem reading Flash across the entire temperature range of -40 °C to 125 °C. This errata does not apply to –A (Automotive Grade) devices.

   Impacts: Flash bits programmed at temperatures below 0 °C might not read back correctly at elevated temperatures.

   Workaround: Program the Flash in production and in-system at 0 °C or higher. If programming must be performed at temperatures lower than 0 °C, a validation of the Flash at 25 °C or greater is highly recommended.

   Resolution: The next revision of the data sheet, revision 1.3, will include a new specification for the valid temperature range to program a device.

2. **Description**: If the /RST pin is held low for more than 1 second while power is applied to the device, and then /RST is released, a percentage of devices may “lock up”, and fail to execute code. Toggling the /RST pin does not clear the condition. The condition is cleared by cycling power. Most devices that are affected will show the lock up behavior only within a narrow range of temperatures (a 5 to 10 degrees C window).

   Impacts: Devices that lock up due to this issue will fail to execute code until the next power-on reset.

   Workaround: Ensure that the reset low time does not exceed 1 second.

   Resolution: Silicon Labs has identified a solution to this problem and this solution has been tested and qualified. Parts with the fix do not have any restrictions on /RST low time. The silicon revision remains the same, but Revision B parts that implement the fix can be identified visually using the assembly date code marking on the device. A four-digit assembly build date code is marked on each part on the bottom-most line. This is in the format YYWW, where YY is the two-digit assembly build calendar year and WW is the two-digit assembly build work week. All parts that have an assembly date code of 1124 or later (year 2011, work week 24) do not have any restrictions on /RST low time.

3. **Description**: If VDD is selected as the voltage reference (REF0CN.3 = 1), and the ADC is enabled (ADC0CN.7 = 1), the P0.0/VREF pin cannot operate as a general purpose I/O pin in open-drain mode. With the above settings, this pin can operate in push-pull output mode or as an analog input.

   Impacts: If the P0.0/VREF pin is configured for open-drain mode with the voltage reference (VREF) set to VDD, the voltage at the pin is indeterminate.

   Workaround: Ensure that the P0.0 pin is not used in open-drain mode as an input or output.

   Resolution: The next revision of the data sheet, revision 1.3, will indicate that the conditions under which the P0.0/VREF pin should not be used in open-drain mode.

Note: C8051F5xx products are AEC-Q100 compliant and qualification and fault coverage reports are available upon request. A list of Silicon Laboratories sales representatives can be found at www.silabs.com. The next revision of the device datasheet will include this note in the relevant sections.