QUAD CHANNEL M-LVDS RECEIVERS

Check for Samples: SN65MLVD048

FEATURES

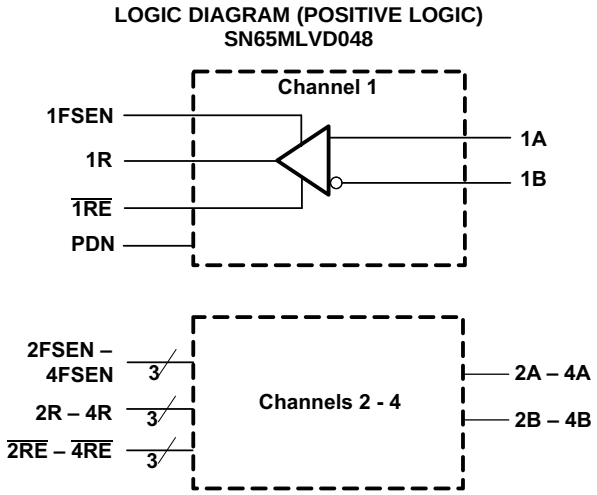
- **Low-Voltage Differential 30-Ω to 55-Ω Line Receivers for Signaling Rates(1) up to 250Mbps; Clock Frequencies up to 125MHz**
- **Type-1 Receiver Incorporates 25 mV of Input Threshold Hysteresis**
- **Type-2 Receiver Provides 100 mV Offset Threshold to Detect Open-Circuit and Idle-Bus Conditions**
- **Wide Receiver Input Common-Mode Voltage Range, –1 V to 3.4 V, Allows 2 V of Ground Noise**
- **Meets or Exceeds the M-LVDS Standard TIA/EIA-899 for Multipoint Topology**
- **High Input Impedance when V_{cc} ≤ 1.5V**
- **Enhanced ESD Protection: 7 kV HBM on all pins**
- **48-Pin 7 X 7 QFN (RGZ)**

(1) The signaling rate of a line is the number of voltage transitions that are made per second, expressed in the units bps (bits per second).

APPLICATIONS

- **Parallel Multipoint Data and Clock Transmission via Backplanes and Cables**
- **Cellular Base Stations**
- **Central Office Switches**
- **Network Switches and Routers**

LOGIC DIAGRAM (POSITIVE LOGIC)



DESCRIPTION

The SN65MLVD048 is a quad-channel M-LVDS receiver. This device is designed in full compliance with the TIA/EIA-899 (M-LVDS) standard, which is optimized to operate at signaling rates up to 250 Mbps. Each receiver channel is controlled by a receive enable ($\overline{RE}$). When $\overline{RE}$ = low, the corresponding channel is enabled; when $\overline{RE}$ = high, the corresponding channel is disabled.

The M-LVDS standard defines two types of receivers, designated as Type-1 and Type-2. Type-1 receivers have thresholds centered about zero with 25 mV of hysteresis to prevent output oscillations with loss of input; Type-2 receivers implement a failsafe by using an offset threshold. Receiver outputs are slew rate controlled to reduce EMI and crosstalk effects associated with large current surges.

The devices are characterized for operation from –40°C to 85°C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
1R—4R	36, 33, 29, 26	O	Data output from receivers
1A–4A	47, 3, 9, 13	I/O	M-LVDS bus non-inverting input/output
1B–4B	48, 4, 10, 14	I/O	M-LVDS bus inverting input/output
GND	6, 7, 18, 23, 27, 31, 34, 38, 43	I	Circuit ground. **ALL GND pins must be connected to ground.**
V_{CC}	2, 11, 15, 16, 24, 37, 45, 46	I	Supply voltage. **ALL VCC pins must be connected to supply.**
$\overline{1RE}$–$\overline{4RE}$	40, 42, 19, 21	I	Receiver enable, active low, enables individual receivers. When this pin is left floating, internally this pin will be pulled to logic HIGH.
1FSEN–4FSEN	39, 41, 20, 22	I	Failsafe enable pin. When this pin is left floating, internally this pin will be pulled to logic HIGH. This pin enables the Type 2 receiver for the respective channel. xFSEN = L → Type 1 receiver inputs xFSEN = H → Type 2 receiver inputs
PDN	30		Power Down pin. When this pin is left floating, internally this pin will be pulled to logic LOW. When PDN is HIGH, the device is powered up. When PDN is LOW, the device overrides all other control and powers down. All outputs are Hi-Z
NC	1, 5, 8, 12, 17, 25, 28, 32, 35		Not Connected
NC	44		Not Connected. Internal TI Test pin. **This pin must be left unconnected.**
PowerPAD™	–		Connected to GND

RGZ PACKAGE
(TOP VIEW)

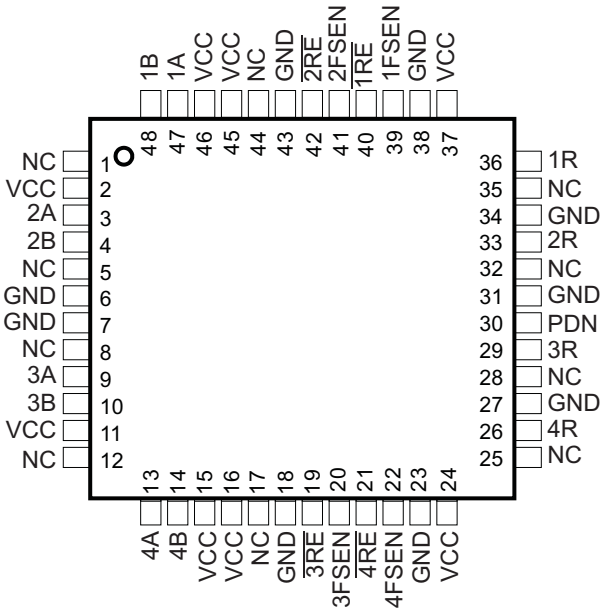


Table 1. DEVICE FUNCTION TABLE

INPUTS[1]				RECEIVER TYPE	OUTPUT[1]
$V_{ID} = V_A - V_B$	PDN	FSEN	$\overline{RE}$		R
V_{ID} > 35 mV	H	L	L	Type 1	H
–35 mV ≤ V_{ID} ≤ 35 mV	H	L	L	Type 1	?
V_{ID} < – 35 mV	H	L	L	Type 1	L
V_{ID} > 135 mV	H	H	L	Type 2	H
65 mV ≤ V_{ID} ≤ 135 mV	H	H	L	Type 2	?
V_{ID} < 65 mV	H	H	L	Type 2	L
Open Circuit	H	L	L	Type 1	?
Open Circuit	H	H	L	Type 2	L
X	H	X	H	X	Z
X	H	X	OPEN	X	Z
X	L	X	X	X	Z

(1) H=high level, L=low level, Z=high impedance, X=Don't care, ?=indeterminate

ORDERING INFORMATION[1]

PART NUMBER	FUNCTION	PART MARKING	PACKAGE / CARRIER
SN65MLVD048RGZR	M-LVDS Type 1 and 2 Receiver	MLVD048	48-Pin QFN / Tape and Reel
SN65MLVD048RGZT		MLVD048	48-Pin QFN / Small Tape and Reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PACKAGE DISSIPATION RATINGS[1]

PACKAGE	PCB TYPE	T_A ≤ 25°C POWER RATING	DERATING FACTOR[2] ABOVE T_A = 25°C	T_A = 85°C POWER RATING
48-Pin QFN (RGZ)	Low-K	1298 mW	12.98 mW/°C	519 mW
	High-K	3448 mW	34.48 mW/°C	1379 mW

(1) The thermal dissipations are in the consideration of soldering down the powerPAD without via on each type of boards.
(2) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

THERMAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance			9		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			20		°C/W
$R_{\theta JP}$	Junction-to-pad thermal resistance			1.37		°C/W
P_D	Device power dissipation	$\overline{RE}$ at 0 V, C_L = 15 pF, V_{ID} = 400 mV, 125 MHz			339	mW

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

				VALUE	UNIT
V_{CC}	Supply voltage range(2)			–0.5 to 4	V
	Input voltage range	$\overline{RE}$, FSEN		–0.5 to 4	V
		A or B		–1.8 to 4	V
	Output voltage range	R		–0.3 to 4	V
	Electrostatic discharge	Human-body model(3)	All other pins	±7	kV
		Charged-device model(4)	All pins	±1.5	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-E. Bus pin stressed with respect to a common connection of GND and V_{CC}.
(4) Tested in accordance with EIA-JEDEC JESD22-C101D.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	GND		0.8	V
V_A or V_B	Voltage at any bus terminal	–1.4		3.8	V
$\|V_{ID}\|$	Magnitude of differential input voltage	0.05		V_{CC}	V
V_{IC}	Differential common-mode input voltage	–1		3.4	V
R_L	Differential load resistance	30	50		Ω
$1/t_{UI}$	Signaling rate			250	Mbps
T_A	Operating free-air temperature	–40		85	°C

DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current	$\overline{RE}$ at 0 V for all channels C_L = 15 pF, V_{ID} = 400 mV, 125 MHz		86	94	mA
	Power down	PDN = L		0.75	1.5	mA

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold	Type 1	See Table 2 and Table 3			35	mV
		Type 2				135	
V_{IT-}	Negative-going differential input voltage threshold	Type 1		–35			mV
		Type 2		65			
V_{HYS}	Differential input voltage hysteresis ($V_{IT+} – V_{IT-}$)	Type 1			25		mV
		Type 2			0		
V_{OH}	High-level output voltage		I_{OH} = –8 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 8 mA			0.4	V
I_{IH}	High-level input current		V_{IH} = 2 V to V_{CC}	–10			µA
I_{IL}	Low-level input current		V_{IL} = GND to 0.8 V	–10			µA
I_{OZ}	High-impedance output current		V_O = 0 V or V_{CC}	–10		15	µA
I_A or I_B	Receiver input current		One input (V_A or V_B) = –1.4 V or 3.8 V, Other input = 1.2 V	–20		20	µA
I_{AB}	Receiver differential input current ($I_A – I_B$)		$V_A = V_B$ = –1.4 V or 3.8 V	–4		4	µA
$I_{A(OFF)}$ or $I_{B(OFF)}$	Receiver input current		One input (V_A or V_B) = –1.4 V or 3.8 V, Other input = 1.2 V, V_{CC} = GND or 1.5 V	–32		32	µA
$I_{AB(OFF)}$	Receiver power-off differential input current ($I_A – I_B$)		$V_A = V_B$ = –1.4 V or 3.8 V, V_{CC} = GND or 1.5 V	–4		4	µA
C_A or C_B	Input capacitance		V_I = 0.4sin(30E6πt) + 0.5V,(2) Other input at 1.2 V		5		pF
C_{AB}	Differential input capacitance		V_{AB} = 0.4sin(30E6πt) + 0.5 V(2)			3	pF
$C_{A/B}$	Input capacitance balance, (C_A/C_B)			0.99		1.01	

(1) All typical values are at 25°C and with a 3.3-V supply voltage.
(2) HP4194A impedance analyzer (or equivalent)

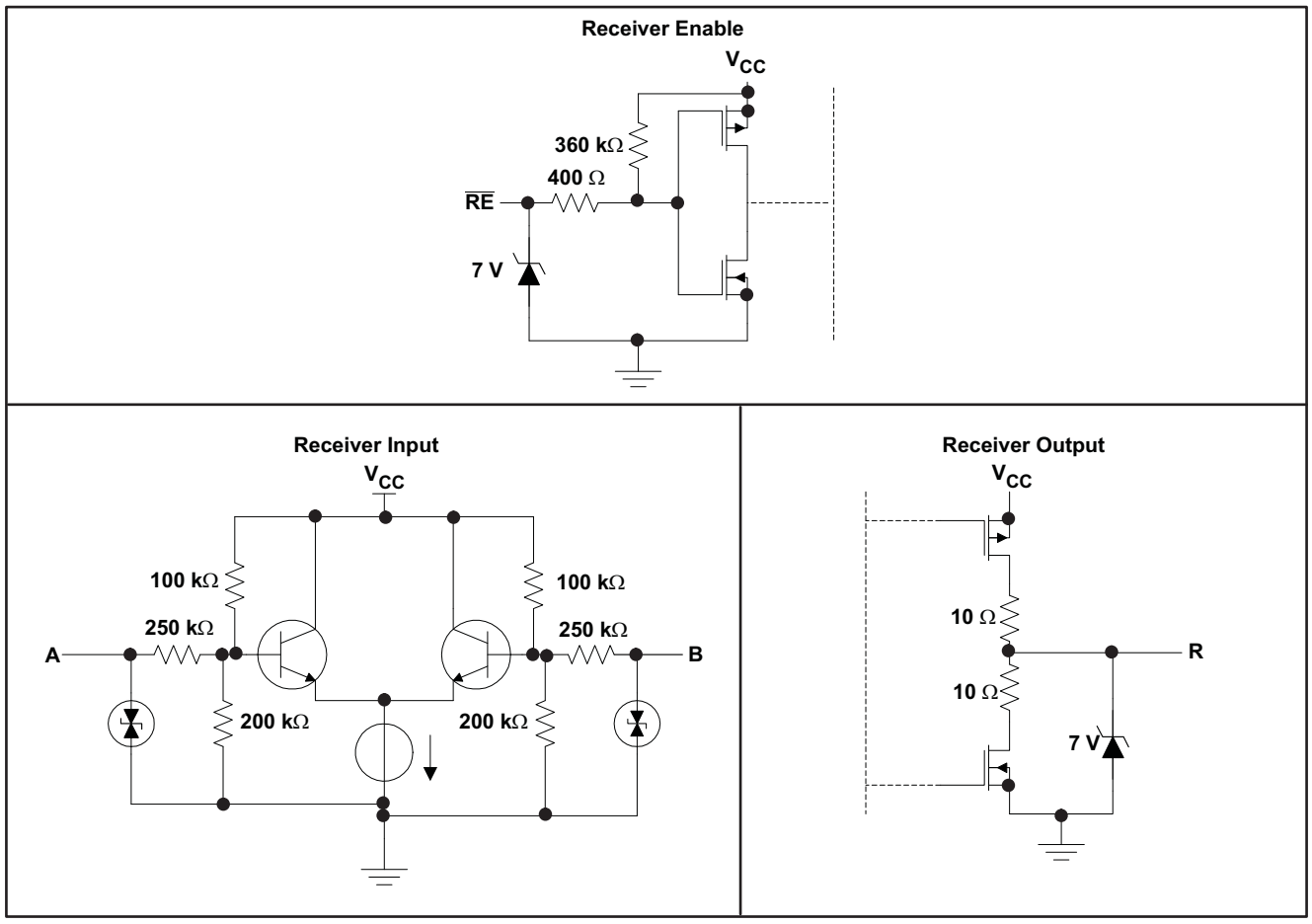
RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		C_L = 15 pF, See Figure 2	2		6	ns
t_{PHL}	Propagation delay time, high-to-low-level output			2		6	ns
t_r	Output signal rise time			1		2.3	
t_f	Output signal fall time			1		2.3	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	Type 1			35	270	ps
		Type 2			150	460	
$t_{sk(pp)}$	Part-to-part skew					800	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation)(2)		All channels switching, 125 MHz clock input(3), See Figure 4			6	ps
$t_{jit(c-c)}$	Cycle-to-cycle jitter, rms(2)					13	ps
$t_{jit(det)}$	Deterministic jitter(2)	Type 1	All channels switching, 250 Mbps 2^{15}-1 PRBS input(3), See Figure 4			800	ps
		Type 2				945	ps
$t_{jit(ran)}$	Random jitter(2)	Type 1				9	ps
		Type 2				8	ps
t_{PZH}	Enable time, high-impedance-to-high-level output		C_L = 15 pF, See Figure 3			15	ns
t_{PZL}	Enable time, high-impedance-to-low-level output		C_L = 15 pF, See Figure 3			15	ns
t_{PHZ}	Disable time, high-level-to-high-impedance output		C_L = 15 pF, See Figure 3			10	ns
t_{PLZ}	Disable time, low-level-to-high-impedance output		C_L = 15 pF, See Figure 3			10	ns

(1) All typical values are at 25°C and with a 3.3-V supply voltage.
(2) Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.
(3) $t_r = t_f$ = 0.5ns (10% to 90%)

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



PARAMETER MEASUREMENT INFORMATION

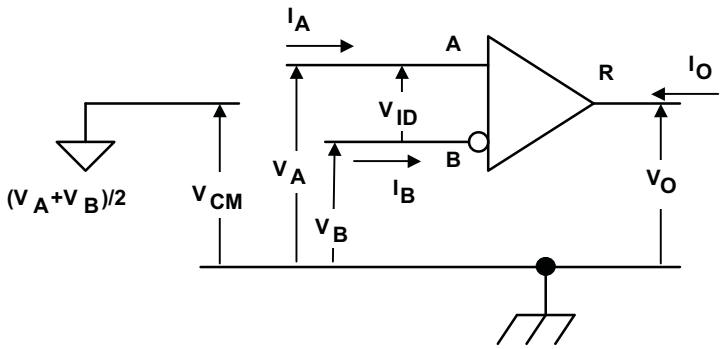


Figure 1. Receiver Voltage and Current Definitions

Table 2. Type-1 Receiver Input Threshold Test Voltages

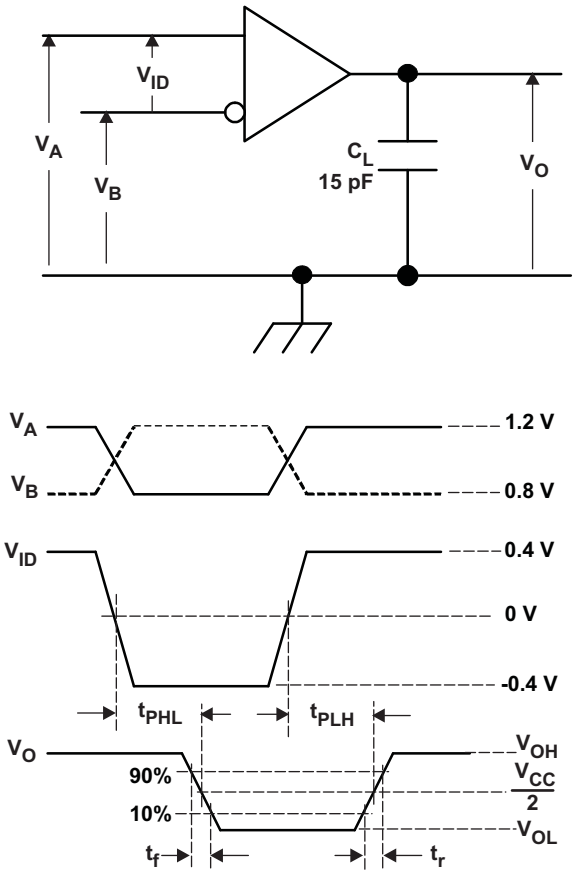
APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	RECEIVER OUTPUT(1)
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	–2.400	1.200	L
3.400	3.365	0.035	3.3825	H
3.365	3.400	–0.035	3.3825	L
–0.965	–1	0.035	–0.9825	H
–1	–0.965	–0.035	–0.9825	L

(1) H= high level, L = low level, output state assumes receiver is enabled ($\overline{RE}$ = L)

Table 3. Type-2 Receiver Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	RECEIVER OUTPUT(1)
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	–2.400	1.200	L
3.400	3.265	0.135	3.3325	H
3.4000	3.335	0.05065	3.3675	L
–0.865	–1	0.135	–0.9325	H
-0.935	–1	0.065	–0.9675	L

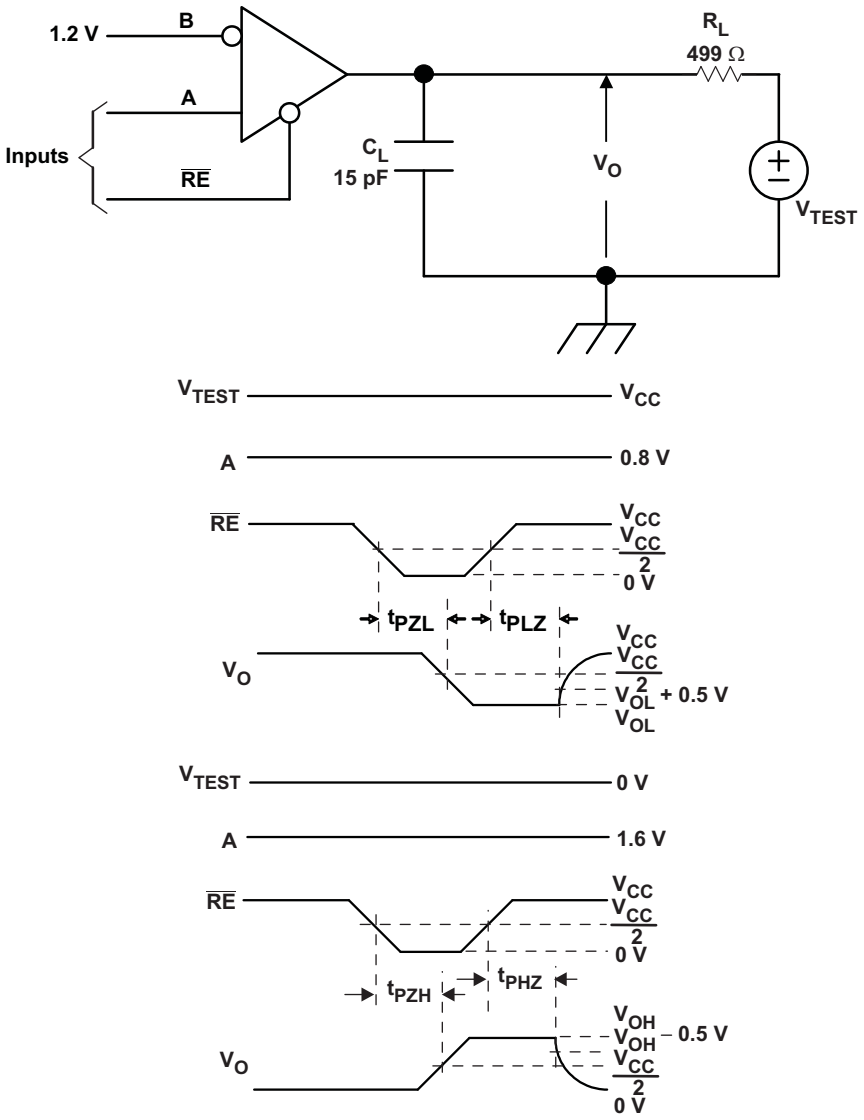
(1) H= high level, L = low level, output state assumes receiver is enabled ($\overline{RE}$ = L)



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, Frequency = 1 MHz, duty cycle = 50 ± 5%. C_L is a combination of a 20%-tolerance, low-loss ceramic, surface-mount capacitor and fixture capacitance within 2 cm of the D.U.T.

B. The measurement is made on test equipment with a –3dB bandwidth of at least 1 GHz.

Figure 2. Receiver Timing Test Circuit and Waveforms

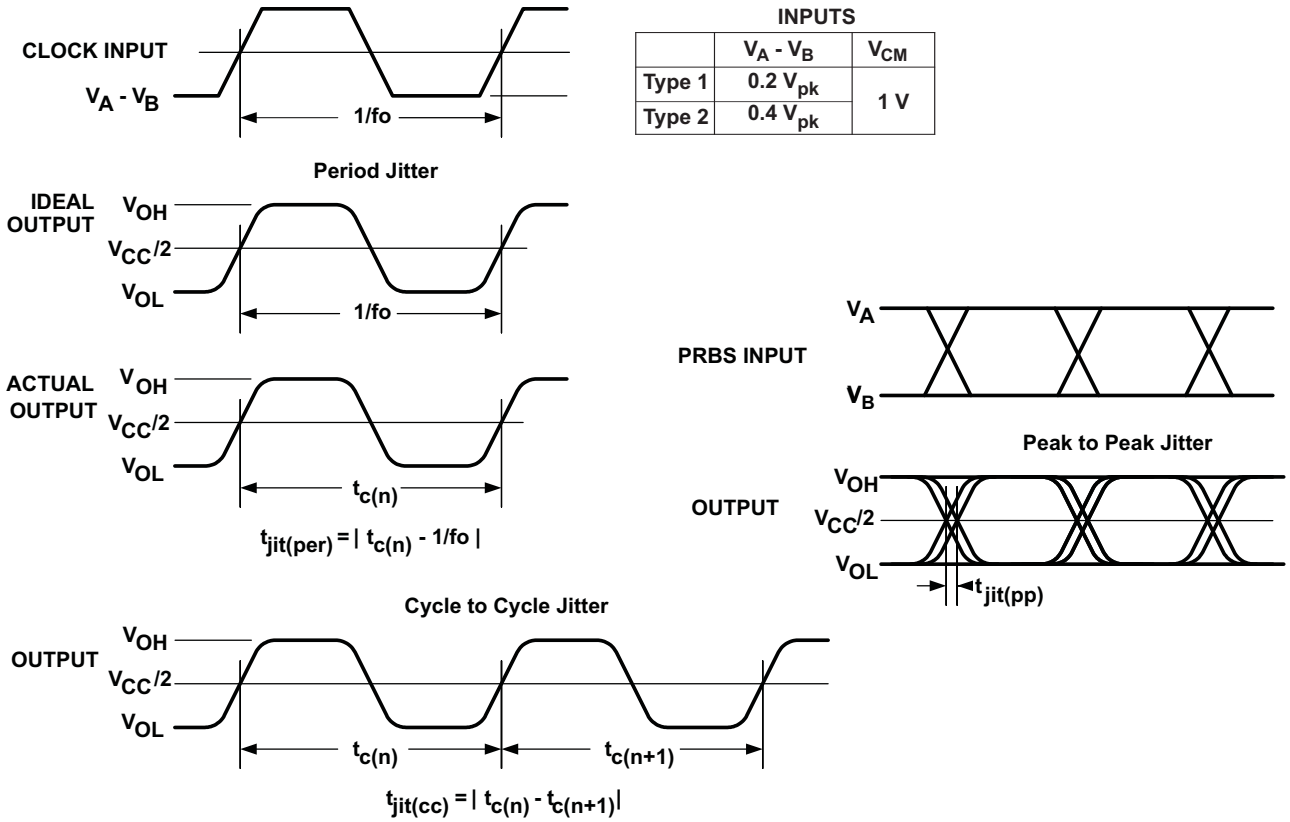


A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, frequency = 1 MHz, duty cycle = 50 ± 5%.

B. R_L is 1% tolerance, metal film, surface mount, and located within 2 cm of the D.U.T

C. C_L is the instrumentation and fixture capacitance within 2 cm of the D.U.T. and ±20%. The measurement is made on test equipment with a –3dB bandwidth of at least 1GHz.

Figure 3. Receiver Enable/Disable Time Test Circuit and Waveforms



A. All input pulses are supplied by the Agilent 81250 Parallel BERT Stimulus System with plug-in E4832A.

B. The cycle-to-cycle jitter measurement is made on a TEK TDS6604 running TDSJIT3 application software.

C. All other jitter measurements are made with an Agilent Infiniium DCA-J 86100C Digital Communications Analyzer.

D. Period jitter and cycle-to-cycle jitter are measured using a 125-MHz 50 ± 1% duty cycle clock input. Measured over 75K samples.

E. Deterministic jitter and random jitter are measured using a 250-Mbps $2^{15\ -1}$ PRBS input. Measured over BER = $10^{\ -12}$

Figure 4. Receiver Jitter Measurement Waveforms

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREQUENCY

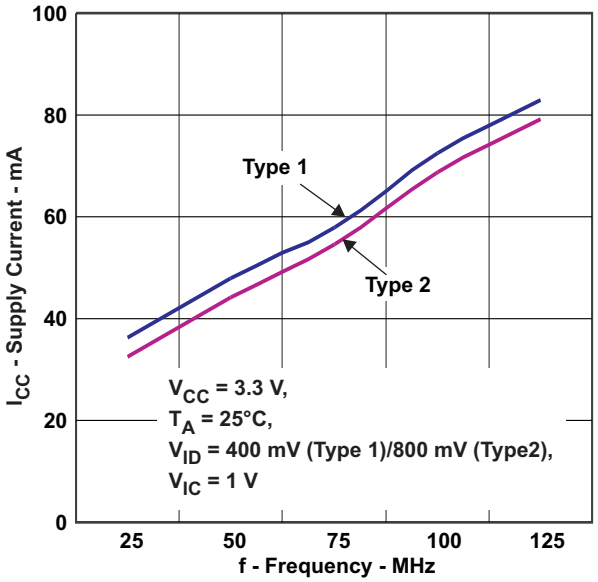


Figure 5.

RECEIVER (TYPE-1) PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

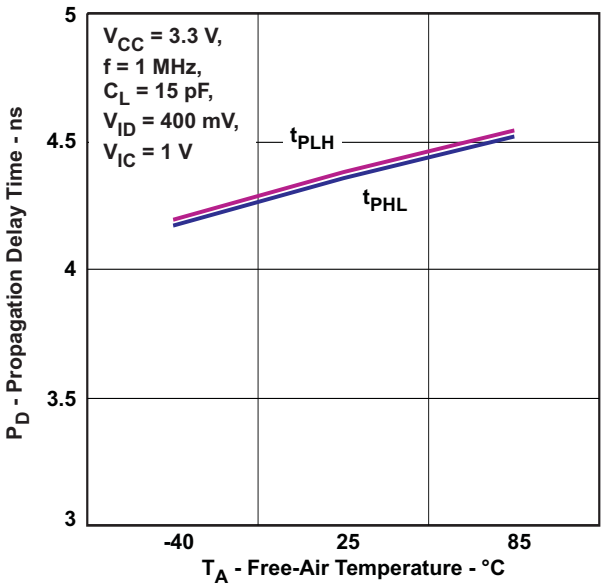


Figure 6.

RECEIVER (TYPE-2) PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

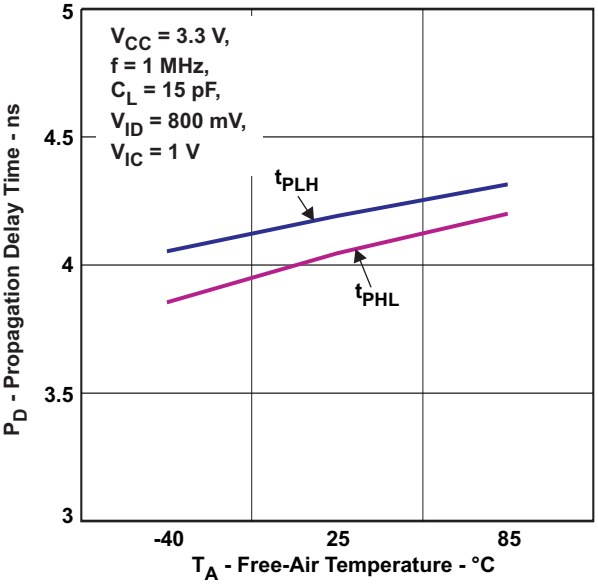


Figure 7.

RECEIVER (TYPE-1) TRANSITION TIME
vs
FREE-AIR TEMPERATURE

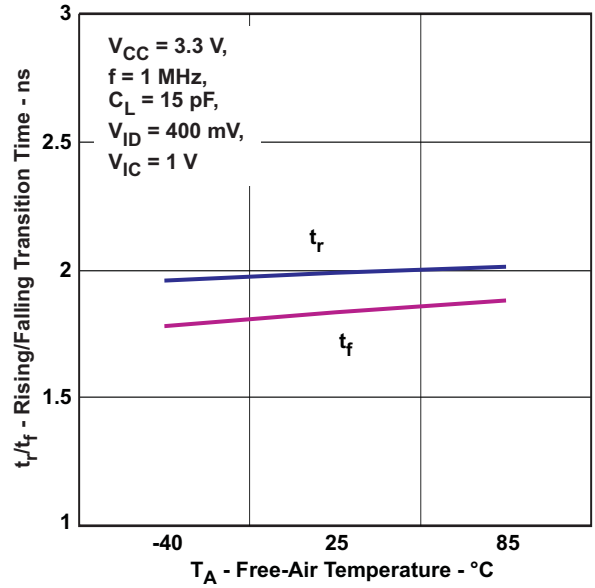


Figure 8.

TYPICAL CHARACTERISTICS (continued)

RECEIVER (TYPE-2) TRANSITION TIME
vs
FREE-AIR TEMPERATURE

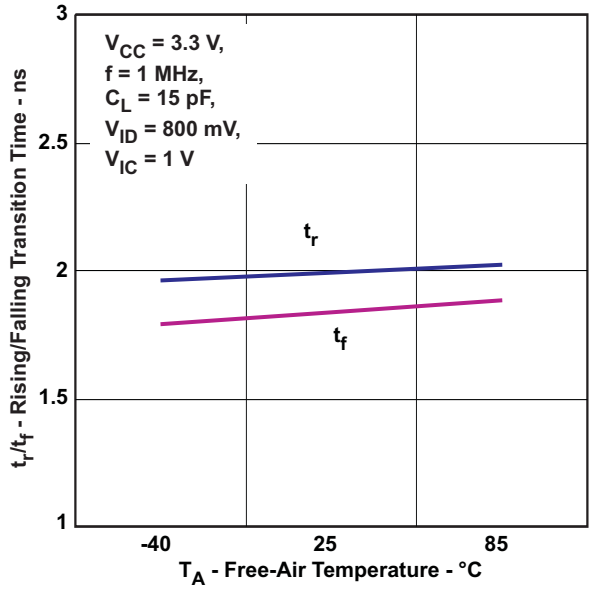


Figure 9.

RECEIVER (TYPE-1) TRANSITION TIME
vs
OUTPUT LOAD CAPACITOR

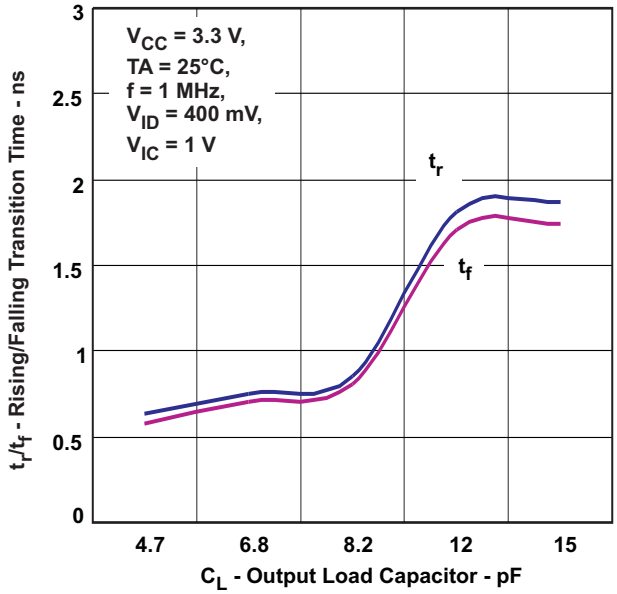


Figure 10.

RECEIVER (TYPE-2) TRANSITION TIME
vs
OUTPUT LOAD CAPACITOR

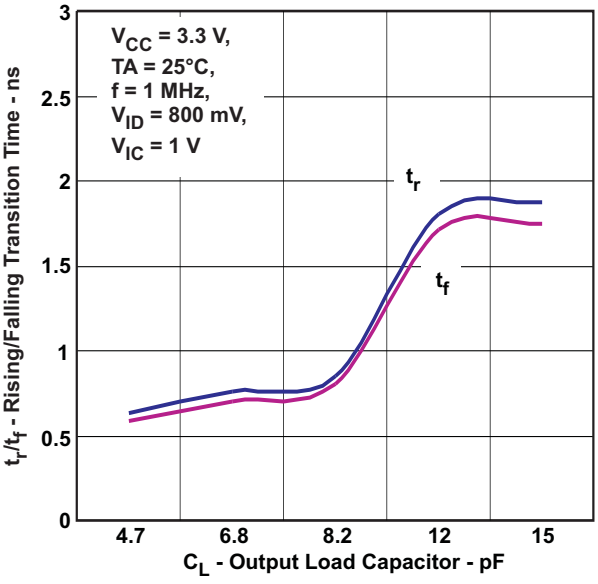


Figure 11.

ADDED RECEIVER PEAK-TO-PEAK JITTER
vs
SIGNALING RATE

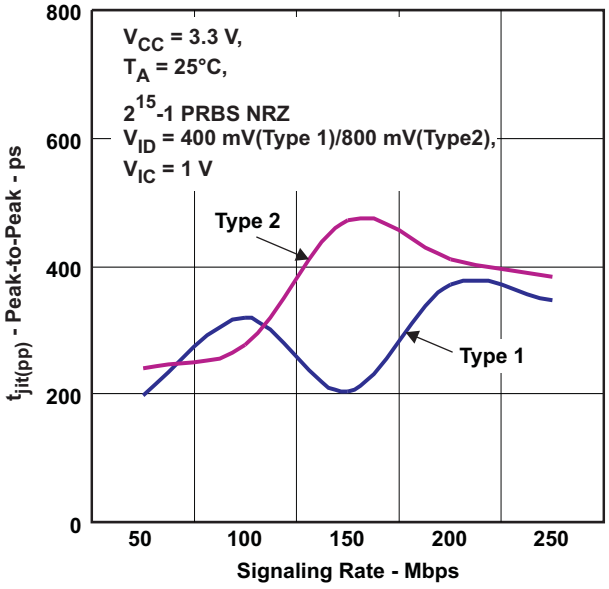


Figure 12.

TYPICAL CHARACTERISTICS (continued)

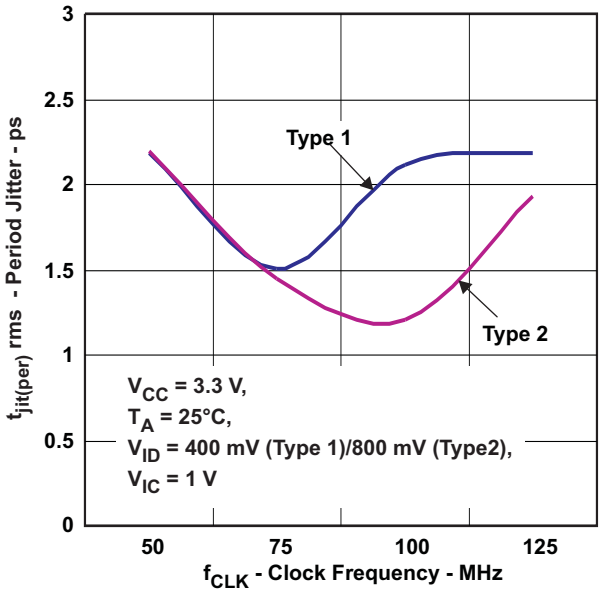


Figure 13.

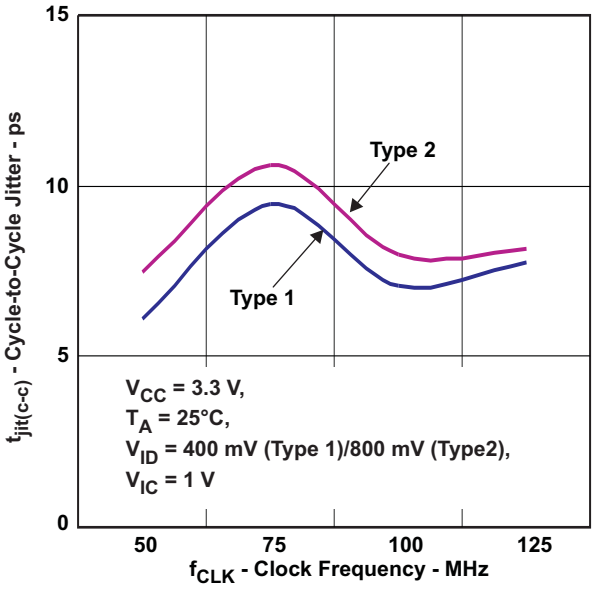


Figure 14.

EYE PATTERNS

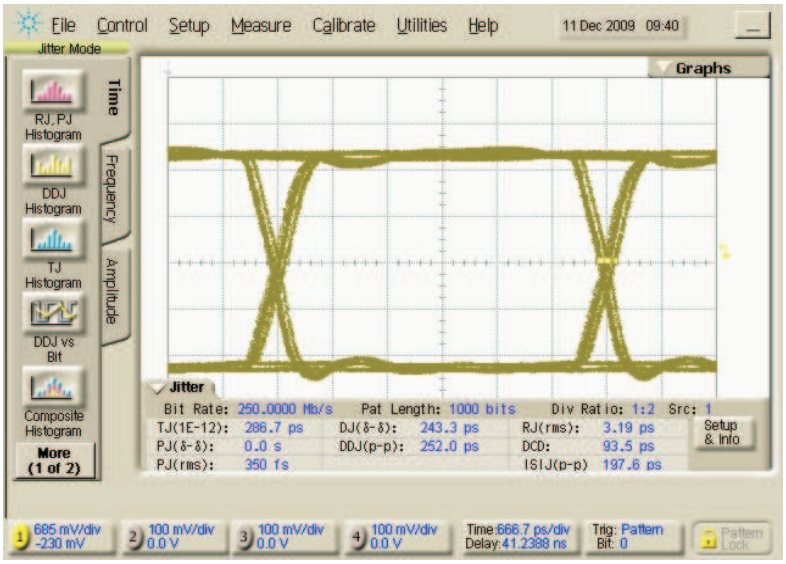


Figure 15. SN65MLVD048 Output (V_{CC} = 3.3 V, V_{ID} = 400 mV) 250 Mbps 2^{15}–1 PRBS, Receiver Type 1

TYPICAL CHARACTERISTICS (continued)

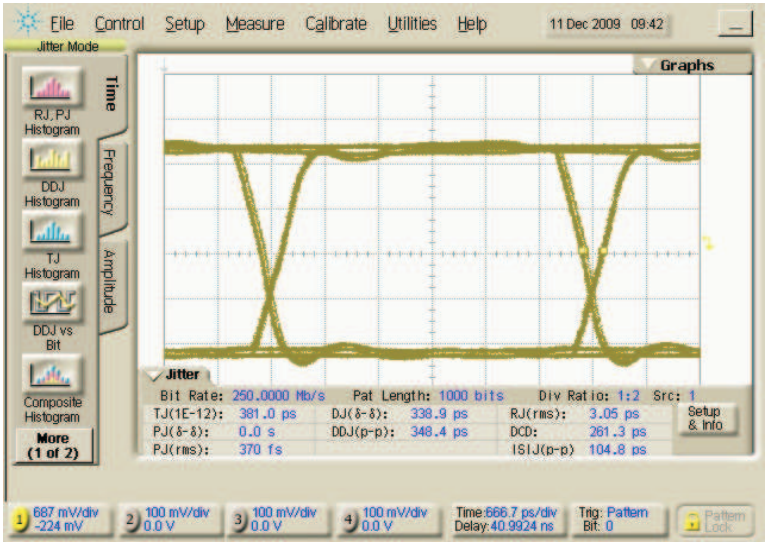


Figure 16. SN65MLVD048 Output (V_{CC} = 3.3 V, V_{ID} = 800 mV) 250 Mbps 2^{15}–1 PRBS, Receiver Type 2

PACKAGING INFORMATION

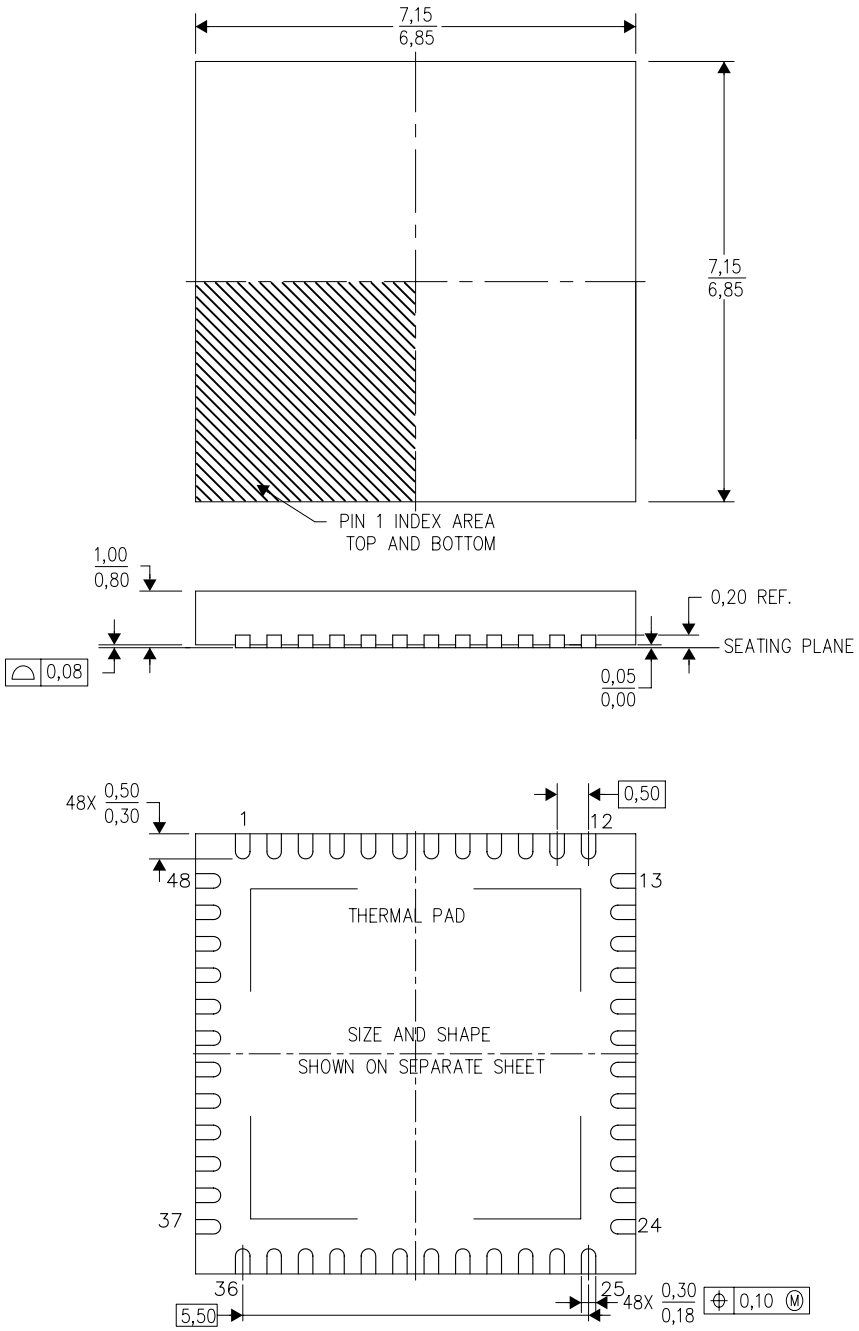
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65MLVD048RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
SN65MLVD048RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

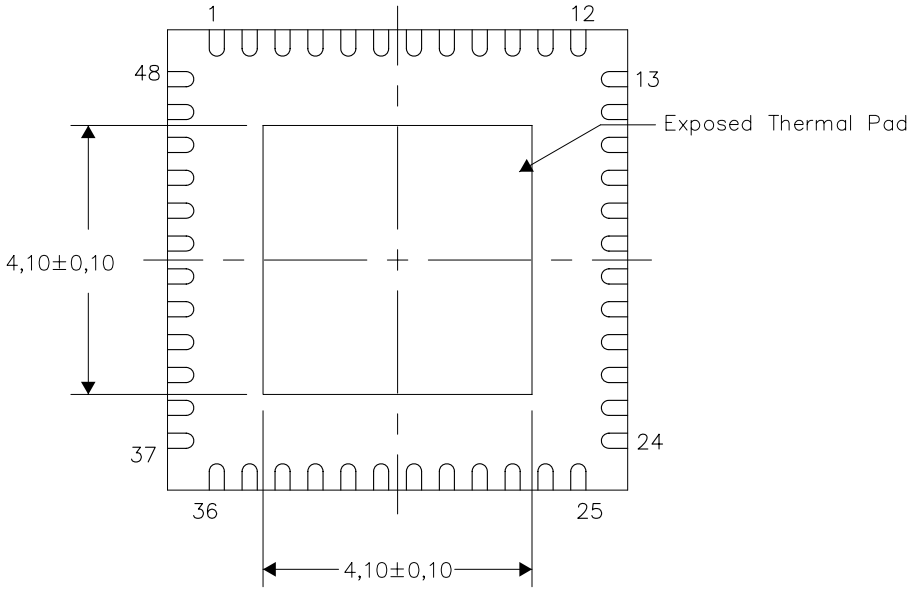
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



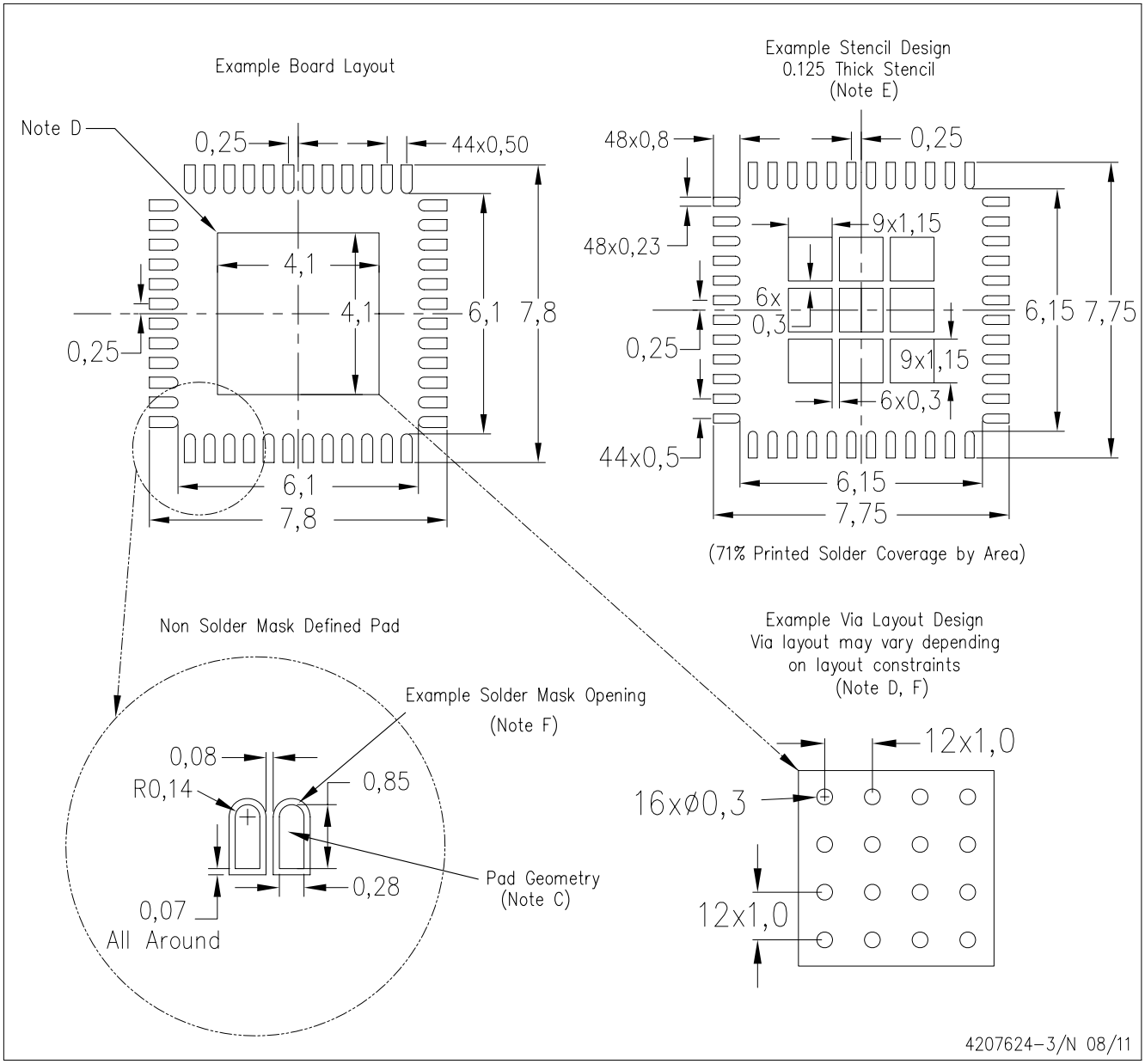
Bottom View

Exposed Thermal Pad Dimensions

4206354–3/R 08/11

NOTE: All linear dimensions are in millimeters

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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